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A CONDITIONAL SAMPLING MODULE FOR THE TSI LASER DOPPLER ANEMOMETER COUNTER PROCESSOR

by

Warren H. March

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A CONDITIONAL SAMPLING MODULE FOR THE TSI LASER DOPPLER ANEMOMETER COUNTER PROCESSOR

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SUMMARY

A module is described that is fully compatible with TSI Laser Doppler Counter Processors and Interfaces and which, when installed, permits conditional sampling of the TSI Laser Doppler Anemometer Output at some predetermined cyclic or externally imposed rate.

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1. BACKGROUND

Laser Doppler Anemometry (LDA) is a well established flow measurement technique, having the advantages of being non-intrusive and calibration-free, with high spatial and temporal resolution. A significant disadvantage of the technique, however, is the existence of velocity biasing problems associated with highly turbulent flows, and density biasing problems which arise in turbulent combusting flows. The majority of these biases can be eliminated with good optics and frequency shifting of the laser beam.

One bias problem remains, due to the fact that a laser doppler anemometer measures instantaneous velocities of individual particles. Measurement of a large number of particle velocities allows the calculation of statistical quantities that describe the average particle flow. However, turbulent flow processes are conventionally described in terms of time-averaged velocity components and velocity correlations, which generally differ from the above particle-averaged quantities since, for an uniformly seeded flow, the particle arrival rate is dependent on the flow velocity. Several correction schemes[1,2] have been proposed to remove this bias, but modern techniques tend to favour some form of conditional sampling[3,4,5], such that the velocity sampling of the flow is not controlled by the particle arrival rate. The ability to impose conditional sampling is also of value in synchronizing measurements of velocity with external events having periodicity, such as occur in rotating machinery or reciprocating engines.

A common method for obtaining conditionally sampled data involves recording both the raw data and a synchronizing signal, and post-processing the data according to the required algorithm. However, in a typical LDA measurement the conditioned data might represent less than 1% of validated data points, and the above process can result in unacceptable computational overheads. The device described below enables conditional sampling which is controlled either externally or by an internally generated pulse rate. When the internal pulse rate is used to control sampling, the sampling frequency is set at least 2 orders lower than the particle arrival rate so that the fluid-velocity can be considered to be sampled at fixed intervals and therefore free of bias. Data are passed to the computer at the sampling rather than the particle arrival rate and excessive overheads are therefore avoided.

The device has been designed for use with TSI LDA system and configured for the HP-9825A computer.

2. INTERFACE PRINCIPLES

2.1 Introduction

The ARL 60 105 conditional interface is designed as an add-on component to the TSI 1998 Master Interface, and enables DMA (Direct Memory Access) transfer of the data from the TSI 1998 Master Interface to the Hewlett Packard 9825A Computer via the HP 98032A interface. The general arrangement is shown in Figure 1. Details of operation of the TSI 1990,

HP 98032A and HP 9825A are to be found in relevant manuals[6,7,8]. A brief description only is included here for convenience.

2.2 TSI 1990 Counter

Each time a velocity data point is validated and latched into the output register, the TSI 1990 counter generates the following output:

(a) 16 Bit time output

(b) 8 Bit cycle count output

(c) 1 Bit data ready pulse.

The cycle count plus the time output together determine the doppler frequency, although the latter is sufficient information if the counter is operating in the fixed N cycle mode.

2.3 TSI 1998 Master Interface

The 1998 Master Interface uses the above information to generate two 16 Bit words for each counter in the system and transfers this information in bit parallel, word serial form to the computer. The interface also generates a third word representing time between data points (TBD). the words contain the following information:

(a) Word A: 8 bit cycle count, 2 bit processor address, 1 bit counter mode, 1 bit first transfer after synchronizing pulse.

(b) Word B: 16 bit time output.

(c) Word TBD: 16 bit time between data points.

Three bits are used to control the data transfer handshake between the interface and the computer. The interface will always transmit word B. Words A and TBD are optional.

The interface may operate in one of two modes - random or coincidence. In random mode the interface will transmit data from a counter each time it receives a "data ready" pulse from that counter. In coincidence mode, the data is transferred only if all counters in the system generate a "data ready" pulse within a previously programmed coincidence interval.

2.4 ARL Conditional Interface

The Conditional Interface (Fig. 2) operates in two modes - Active and Internal Rate. In the internal rate mode the data is transferred directly from the master interface to the computer, the sole function of the conditional interface being to enable the correct handshake between the master interface and the computer.

In active mode the sampling frequency is controlled by either an internally or an externally generated square wave in the following manner. During normal operations and upon receipt of a data ready pulse

from the counter, the TSI 1998 interface imposes an inhibit on the TSI 1990 counter to prevent updating of the output registers during the data transfer operation. The circuit has been modified to prevent this inhibit from being cleared until the next rising edge of the sampling frequency square wave following completion of the data transfer. The maximum data rate from the counter is therefore equal to the prescribed sampling frequency although the actual rate may be less than this. The internally generated sampling frequency is periodic and continuously variable in the range of 650 kHz to 0.03 Hz.

The sampling frequency also generates a synchronising pulse which may be inserted in either the internal rate or active mode to enable determination of the temporal relationship between data points and the event generating the synchronizing pulse.

3. CONSTRUCTION AND OPERATIONS

Detailed drawings for the conditional interface are described in ARL Series Parts List No. 60105-A2, portions of which are reproduced in Figure 3.

Figure 4 shows the minor rework necessary to the TSI 1998 interface to enable operation of the conditional interface. Supply voltage for the conditional interface has been connected to Pin 30. A second J-K flip flop (U76) has been inserted in the data hold (counter inhibit) circuit and the data between this flip flop and the original data hold flip flop is formed external to the interface through pins 46 and 50 on connector J2.

A second modification (Fig. 4, U41) was incorporated to correct a logic error that occurred in the TSI 1998 interface when programmed to transfer only Words A and B. In the unmodified condition the 'First after Synch' bit of Word A would latch only on every second validated data transfer from the counter unless more than one data transfer occurred between synchronizing pulses.

A jumper connected between pins 46 and 50 will enable the TSI 1998 interface to operate in its unmodified mode.

Figure 5 shows the timing diagram for a three word data transfer in the conditional sampling mode. This timing diagram should be read in conjunction with relevant interface and computer manuals.[7,8]

Control line 0 (CTL 0) of the 9825A computer is connected to the ST11 line on the conditional interface. This line enables software control of the sampling mode according to the truth table below.

Initiation of a DMA transfer by the computer drives the PCTL line on the 98025A interface high (PCTL set) which subsequently activates the TSI 1998 interface via the COMMAND line.

When the TSI 1990 counter has data to send to the computer it sends the data together with a "data ready" (DR) pulse to the TSI 1998 interface. The interface responds by sending a DATA HOLD (DH2) to the counter, inhibiting further updating by the counter.

		CTL 1 (ST11) LINE	
		TRUE = LOW	FALSE = HIGH
F U N C T O I N S W I T C H	ACTIVE	CONDITIONAL SAMPLING RATE	INTERNAL
	INTERNAL RATE	INTERNAL RATE	INTERNAL RATE
FIG. 2			
		SAMPLING MODE	

The TSI 1998 interface sends a flag pulse to the HP98032A interface which responds with a level change (PCTL CLEAR) and acceptance by the computer of the data. When the computer is ready for the next word PCTL is changed from "CLEAR" to "SET" and the transfer cycle can be repeated.

When the required number of words for the data point have been transmitted by the TSI 1998 interface the CLRDH1 is activated, clearing the master interface and releasing DH1. The next rising edge of the square wave generates CLR DH2 which releases DH2 (DATA HOLD) and the 1990 counter is free to accept a new data point. If the DMA transfer is incomplete the PCTL line will be reset and the cycle repeated.

If the DMA transfer is completed the control line CTL 0 is usually released (B0-00 High) and the counter allowed to run free. If only one word is read per data measurement a further Low-High transition is required on the B0-00 since an alternative circuit is used to clear the Master Interface.

4. CONFIGURATIONS

For operation as outlined in this technical memorandum the following configurations apply.

(a) TSI 2998 Master Interface

Dip switch I.C. Location U25 on PC2605252

Switch No.	State
1	As required
2	As required
3	As required
4	Not used
5	ON
6	OFF
7	ON
8	Not used

Rotary Switch and Dip switch at IC location on PC2605251 to be set as required.

(b) HP98032A interface

The following configuration jumpers are installed to obtain correct logic.

3, 7, 9, B, D

(c) HP9825A Computer

When operating in DMA mode the following considerations apply.

: To transfer M words from peripheral "2" to buffer "ONE" execute eir2,1;tfr2,"ONE",M;eir2,0

: The TSI 1998 and HP98032A use complementary logic. To read a binary word from buffer "ONE" execute the following statement cmprdb"ONE".

5. ACKNOWLEDGEMENT

The author wishes to acknowledge the assistance of Mr G. Forsyth in the design and Mr K. Vaughan in the construction of this circuit.

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2. Roesler, I., Stevenson, W.H. and Thomson H.D., "Investigation of Bias Errors in Laser Doppler Velocimeter Measurements", AFWAL-TR-80-2108 Dec 1980.

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4. Stevenson, W.H., Thomson, H.D. and Gould, R.D., "Laser Velocimeter Measurements and Analysis in Turbulent Flows with Combustion", AFWAL-TR-82-2076 Part II, July 1983.

5. Craig, R.R., Nejad, A.S., Hahn, E.Y. and Schwartzkopf, K.G., "A general approach for obtaining unbiased LDV data in highly turbulent nonreacting and reacting flows". AIAA-84-0366 January 1984.

6. TSI Incorporated Instruction Manual Model 1990 Counter Type Signal processor for Laser Velocimeter.

7. TSI Incorporated P/N 1990165. Instruction Manual Model 1998 Master Interface.

8. Hewlett-Packard 98032A 16-Bit Interface Installation and Service Manual.
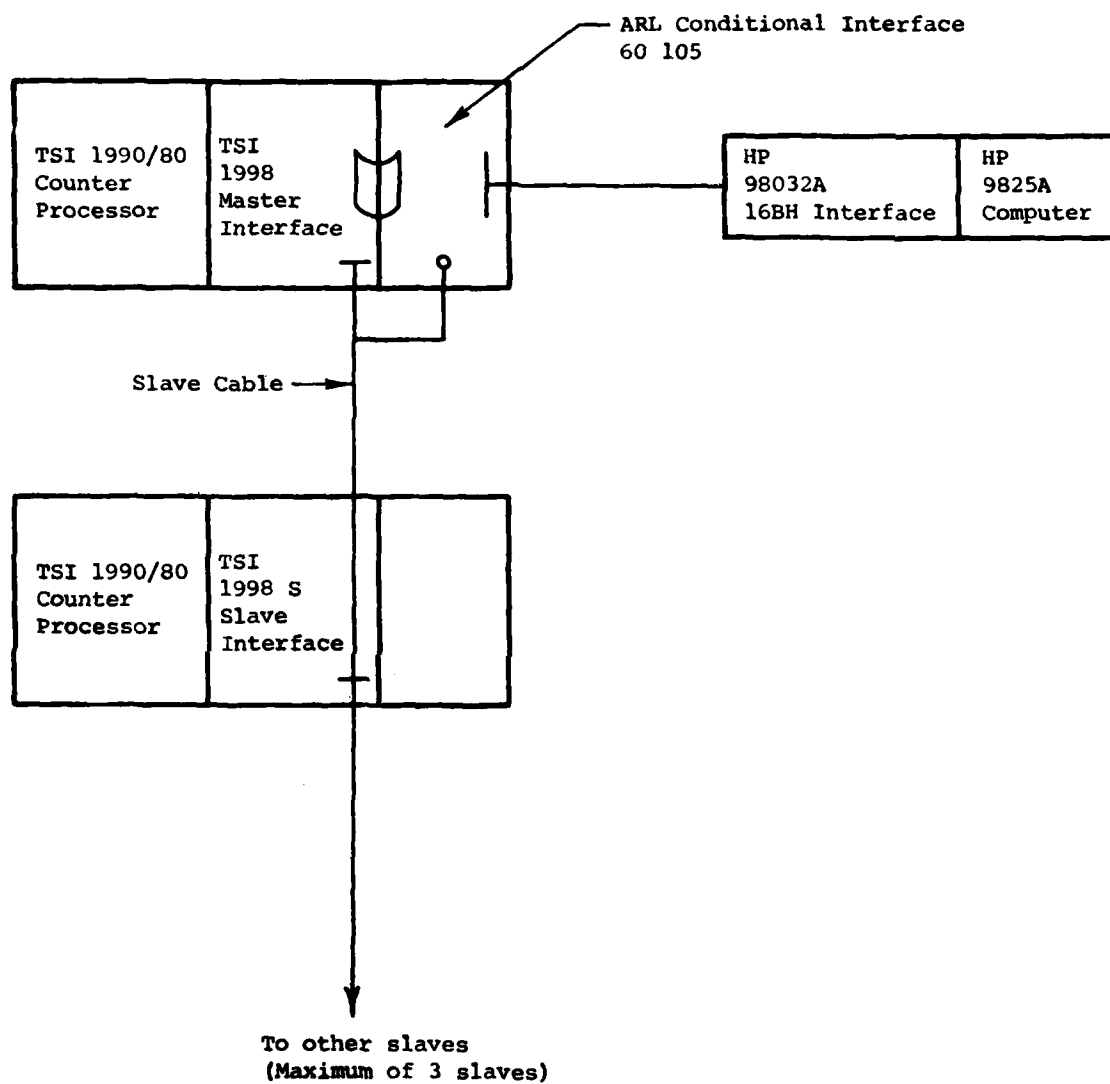
ARL Conditional Interface
60 105

TSI 1990/80 Counter Processor	TSI 1998 Master Interface	

HP 98032A 16BH Interface	HP 9825A Computer

Slave Cable

TSI 1990/80 Counter Processor	TSI 1998 S Slave Interface	

To other slaves
(Maximum of 3 slaves)

FIG. 1   SYSTEM ARRANGEMENT OF COUNTER PROCESSORS, INTERFACES, AND COMPUTER
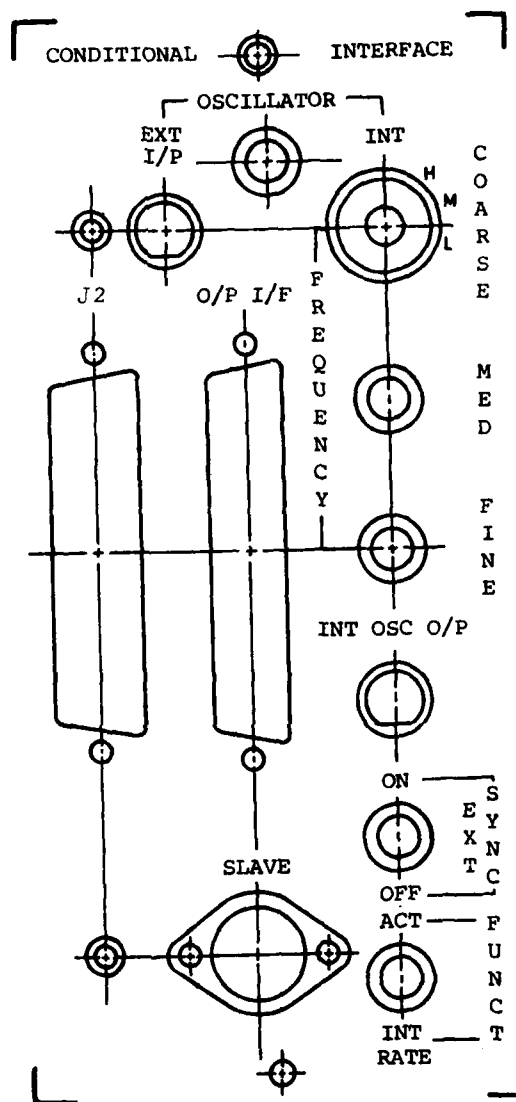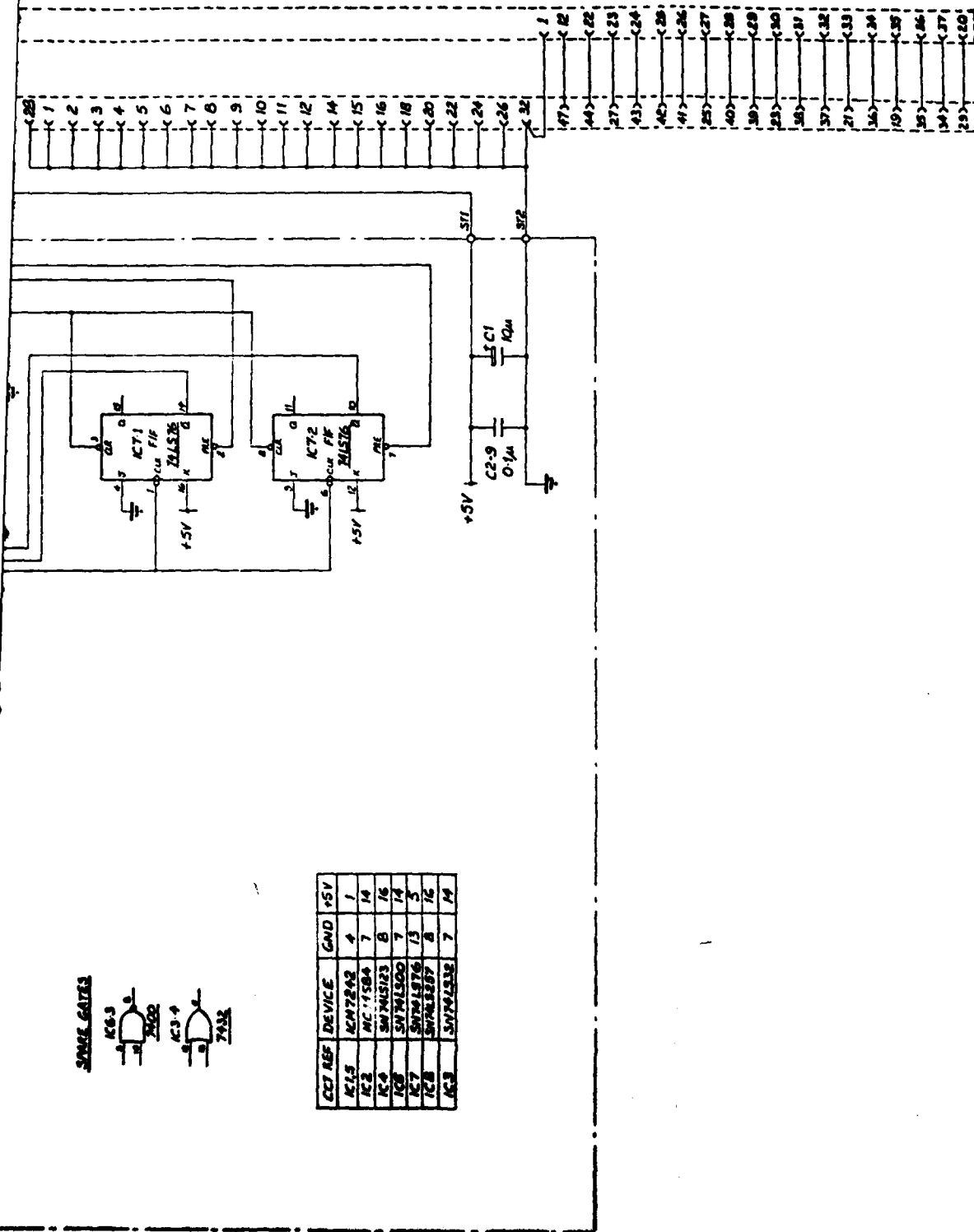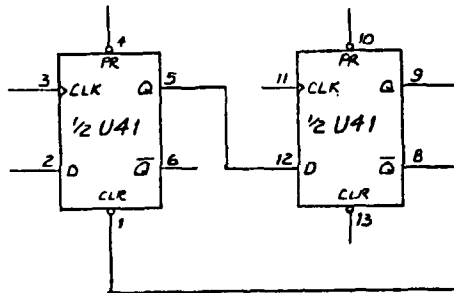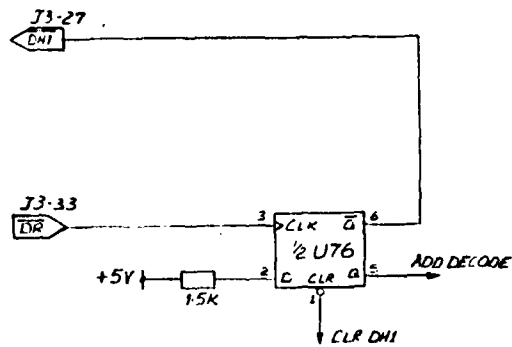
FIG. 2   CONDITIONAL INTERFACE FRONT PANEL
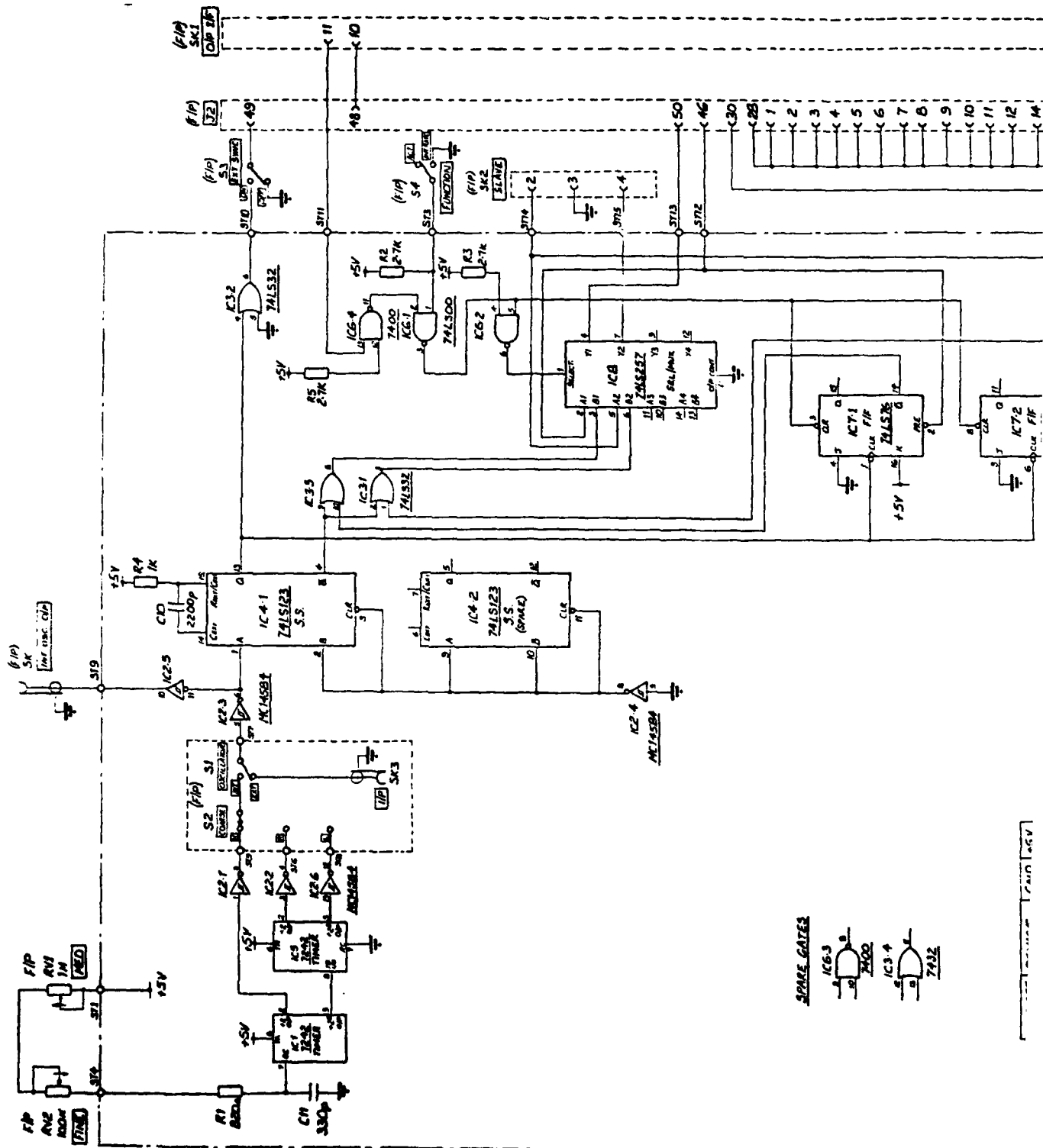
FIG. 3   ARL CONDITIONAL INTERFACE CIRCUIT
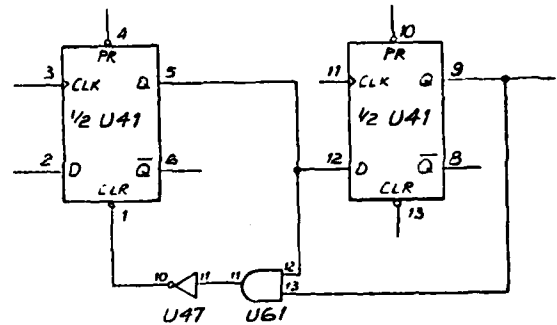
STANDARD CCT IN 1998 M

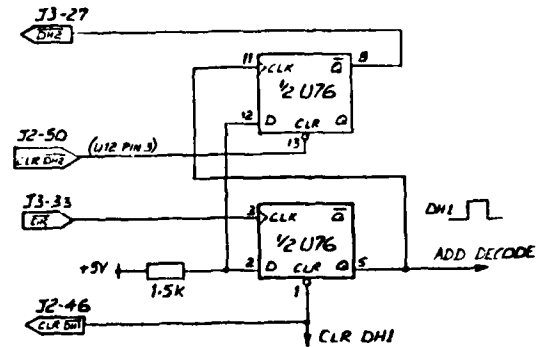MODIFIED CCT FOR 1998 M/S

FIG. 4   TSI 1998 INTERFACE CIRCUIT CHANGES

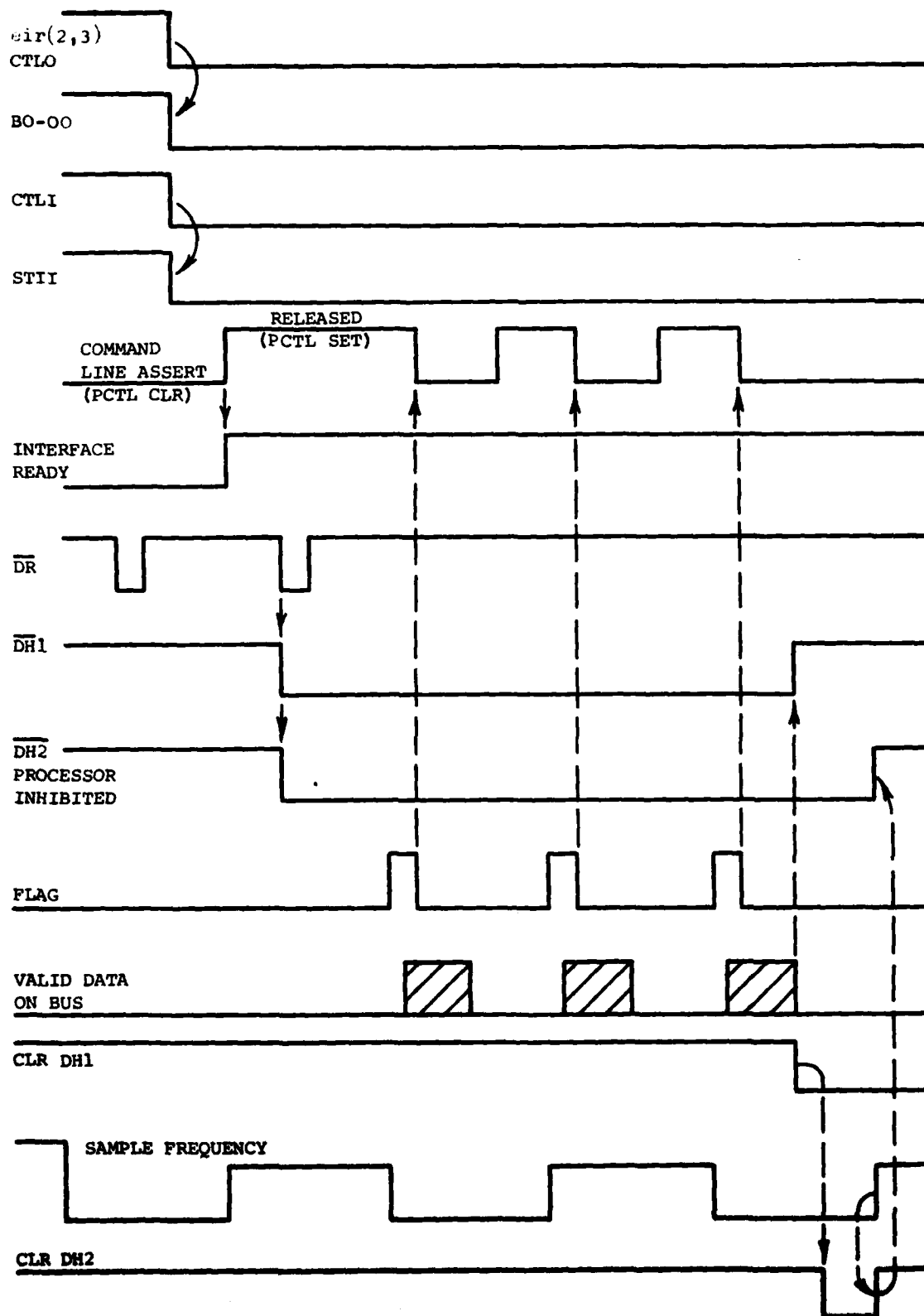FIG. 5   TIMING DIAGRAM FOR A THREE WORD MEASUREMENT
DATA TRANSFER IN CONDITIONAL MODE

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16. Abstract

A module is described that is fully compatible with TSI Laser Doppler Counter Processors and Interfaces and which, when installed, permits conditional sampling of the TSI Laser Doppler Anenometer Output at some predetermined cyclic or externally imposed rate. Keywords;

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